ABSTRACT OF THE DISCLOSURE

Selectively transmitting cache misses within multiple-node shared-memory systems employing coherence protocols is disclosed. A cache-coherent system includes a number of nodes employing a coherence protocol to maintain cache coherency, as well as memory that is divided into a number of memory units. There is a cache within each node to temporarily store contents of the memory units. Each node further has logic to determine whether a cache miss relating to a memory unit should be transmitted to one or more of the other nodes lesser in number than the total number of nodes within the system. This determination is based on whether, to ultimately reach the owning node for the memory unit, such transmission is likely to reduce total communication traffic among the total number of nodes and unlikely to increase latency as compared to broadcasting the cache miss to all the nodes within the system.